

VERTICAL CONDUCTION IN THIN Si/CaF₂/Si STRUCTURES

Jeffrey W. Sleight and Mark A. Reed
 Department of Electrical Engineering, Yale University
 Yale Station, Box 2157
 New Haven, CT 06520

Chih-Chen Cho and Bruce Gnade
 Central Research Laboratory, Texas Instruments
 Dallas, TX

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Electrical characteristics of thin (~100Å), single barrier Si/CaF₂/Si heterostructures have been measured for the first time for both *A* and *B* phase CaF₂. I(V,T) measurements for different thickness CaF₂ barriers show characteristics that are consistent with conduction through defect sites in the CaF₂ layer. The *B*-phase CaF₂ exhibits far more defects than the *A*-phase material. Measurements of different size mesas indicate a defect density on the order of one per 1000µm² in the 100Å barrier thickness *A*-phase material.

1. Introduction

The silicon - calcium fluoride system has long been considered as a candidate for electrical isolation of silicon, especially in the area of 3D device integration.¹ The relatively small 0.6% lattice mismatch at 300°C with Si makes CaF₂ a very promising choice. Additionally, CaF₂ has the attractive property that it can be patterned directly with electron-beam and ion-beam lithography.^{2,3} However, little attention has been given to the transport properties of the Si-CaF₂ heterojunction.

To date, much of the work in this system has either focused on very thick layers (ie. gate dielectrics, >1000Å)⁴ or very thin layers (ie. a few monolayers of CaF₂ on Si). Thin layers of CaF₂ on Si have been studied using a variety of techniques, including; Auger spectroscopy and core level photoemission^{5,6}, medium-energy ion scattering⁷, resonant three-wave-mixing spectroscopy⁸, and transmission electron microscopy.^{9,10} The emphasis of the previous work has been on understanding the electronic and structural properties of the CaF₂/Si interface. Almost all of previously reported work is concerned with exposed CaF₂ layers on top of Si, rather than on a CaF₂ layer buried in Si (ie. a double heterojunction).

Very little attention has been focused on the intermediate regime of a 100-1000Å layer of CaF₂ on Si, or on a heteroepitaxially buried CaF₂ layer. It has been

observed that CaF₂ grows most readily on Si(111) oriented substrates¹¹. On Si(111), two types of growth can occur. Most groups have only observed the growth of *B*-phase.^{12,13,14} Only limited evidence for thin layers of *A*-phase CaF₂ on silicon exists.¹⁰ We have found that we can grow exclusively *A*-phase CaF₂ material by ramping the substrate temperature during growth.¹⁵ The ability to grow *A*-phase CaF₂ may be crucial to achieving good quality films. Figure 1 shows *A*-phase CaF₂ and *B*-phase CaF₂ grown on a stepped Si(111) surface. A Si substrate step in *A*-phase growth can be accommodated, and only creates one dangling F-Ca bond, whereas in *B*-phase growth, the 180° rotation of the CaF₂ lattice in the <111> direction creates line defects at every step site in the silicon substrate.

The growth of thin CaF₂ layers on silicon, and subsequent epitaxial regrowth of silicon, allows the possibility of a heteroepitaxial system in silicon, making heteroepitaxial devices realizable. A few groups have investigated Si/CaF₂/Si structures^{16,17}; however, the thickness of the CaF₂ layer used was rather large (3000-5000Å), which precludes making electron tunneling measurements through these CaF₂ barriers. Given the large conduction band offset of around 2.5eV⁶, the CaF₂ layers will have to be either sufficiently thin and/or possess a light electron effective mass in order to observe a reasonable tunneling current.

In our work, we have examined the simplest possible

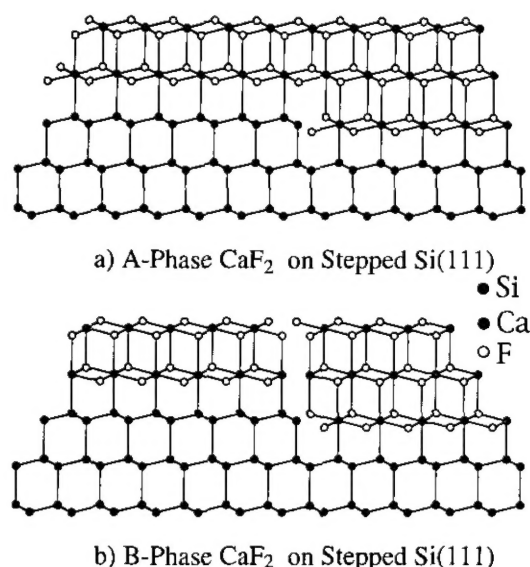


Figure 1: a) Schematic of A-phase CaF_2 on a stepped $\text{Si}(111)$ surface and b) B-phase CaF_2 on a stepped $\text{Si}(111)$ surface. Note the accommodation of the step in the $\text{Si}(111)$ surface in the A-phase CaF_2 versus the gap that forms in the B-phase CaF_2 .

structure in the $\text{Si}/\text{CaF}_2/\text{Si}$ heteroepitaxial system, a single thin barrier of CaF_2 in n-type Si. Ideally, by examining electron transport through CaF_2 barriers of different thicknesses, the conduction band offset and the CaF_2 electron effective mass can be determined. The values obtained in a $\text{Si}/\text{CaF}_2/\text{Si}$ heterostructure for the conduction band offset should be more reliable than those obtained from a measurement on a few monolayers of CaF_2 on top of Si, as the properties of the interface may change substantially when additional monolayers of CaF_2 are present.

2. Growth and Fabrication

The single barrier samples studied were all grown in a VG MBE system. As illustrated in Figure 2, starting with an n-type $\text{Si}(111)$ substrate, a passivating epitaxial layer of n^+ Si (2000 Å to 1 μm thick) was grown via chemical vapor deposition. The sample temperature was then either ramped from 100°C to 600°C for MBE growth of A-phase CaF_2 , or held at 700°C for growth of B-phase CaF_2 . The phase of the CaF_2 was confirmed through x-ray diffraction. A 2000 Å–5000 Å top layer of n^+ silicon was then deposited via CVD. Depending on the growth temperature, the top silicon layer was either single crystalline or polycrystalline.

Devices were fabricated using conventional photolithography and lift-off to create aluminum mesas

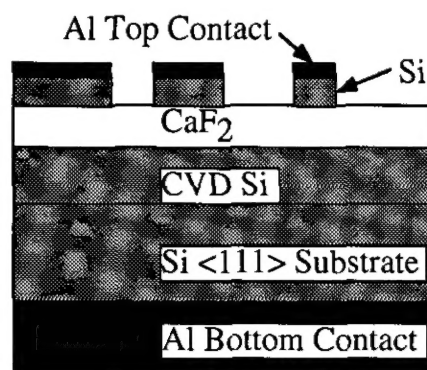


Figure 2: Fabricated device schematic detailing epitaxial layer structure.

which were used as self-aligned etch masks. Mesa size ranged from $8 \times 8 \mu\text{m}^2$ to $256 \times 256 \mu\text{m}^2$. Reactive ion etching was used to remove the top level of silicon. Both SF_6 and CF_4 type reactive ion etching were used, although SF_6 gave better results in terms of creating devices with lower leakage. CaF_2 was observed to serve as an excellent etch stop for SF_6 reactive ion etching. Best results were obtained for using a low power (typically 25 Watts) etch, while flowing 25 SCCM of SF_6 , and maintaining a pressure of 100 mTorr. Electrical contact was made from the mesa top to the backside.

3. Experimental Results

A series of devices was studied to determine differences in the electrical quality of A versus B phase CaF_2 . Nominally identical structures were grown with CaF_2 barrier layers of 100 Å, 200 Å, and 500 Å in thickness. In these devices, the top silicon layer was polycrystalline. As anticipated, the B-phase devices exhibited far worse characteristics than the A-phase devices, with currents several orders of magnitude higher for identical size devices. This is most likely due to the inability of B-phase CaF_2 to compensate for steps in the Si surface, resulting in line defects and pinholes occurring everywhere a step in the Si substrate occurs. This process is illustrated in Figure 1. Additionally, at the growth temperature for B-phase CaF_2 the lattice mismatch is 2.1%, which is much higher than the value of 0.7% where A-phase growth is started. The increase in strain with increasing growth temperature may also play an important role in defect formation.

Figure 3 and 4 show experimental current versus voltage characteristics for a 100 Å and 200 Å layer of A-phase CaF_2 respectively, for four different size devices ($256 \times 256 \mu\text{m}$, $128 \times 128 \mu\text{m}$, $64 \times 64 \mu\text{m}$, and $32 \times 32 \mu\text{m}$). These are typical results from a sampling of 10 devices. Several features are apparent. First, an irrecoverable breakdown was suffered at a field of

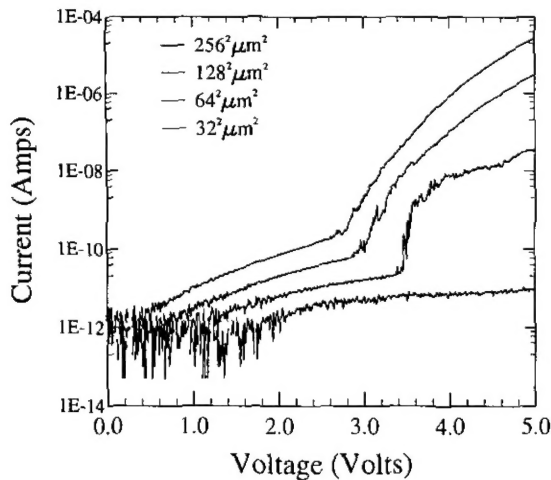


Figure 3: Current versus voltage characteristics for a 100Å A-phase CaF_2 barrier device for different area mesas. $T=300\text{K}$.

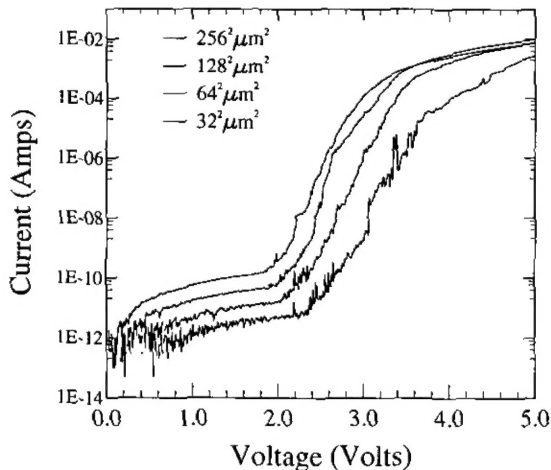


Figure 4: Current versus voltage characteristics for a 200Å A-phase CaF_2 barrier device for different area mesas. $T=300\text{K}$.

around 3×10^6 V/cm (3 volts) in the 100Å sample, and at around 1×10^6 V/cm (2 volts) in the 200Å sample. We believe that this trend of lower breakdown fields in thicker layers is consistent with increasing defect formation due to the increased strain in the thicker layer. However, another possible explanation could be that the thinner layers are better able to dissipate heat than the thicker layers, leading to thermally induced breakdown of the thicker layers at lower fields in comparison to the thinner layers. The smallest device measured in the

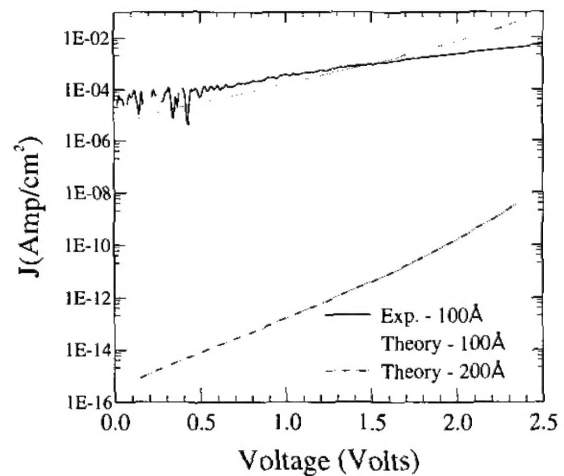


Figure 5: Theoretical current versus voltage curves for a 100Å and 200Å CaF_2 barrier device. $T=300\text{K}$. Experimental data shown (solid line) for 100Å A-phase CaF_2 .

100Å CaF_2 layer exhibited no breakdown until a field of around 7×10^6 V/cm, which is consistent with the dielectric breakdown of CaF_2 ¹⁸, rather than a breakdown process via defects. This implies a defect density of around one per $1000 \mu\text{m}^2$ in the 100Å A-phase CaF_2 .

Although results in the A-phase devices in the low bias regime are more promising than in the B-phase devices, they are still not consistent with tunneling through an epitaxial layer. This is seen by considering the 100Å and 200Å devices. The currents scale with area in the lower bias regime, as expected. However, as shown in Figure 5, theoretical calculations of the tunneling currents in Si/ CaF_2 /Si structures with a thickness of 100Å and 200Å show currents that are nine orders of magnitude different in the lower bias regime, while the experimental curves for both the 100Å and 200Å device have currents that are on the same order of magnitude. The solid line in Figure 5 shows the experimental data for a 100Å A-phase CaF_2 device (the data for a 200Å device would lie almost directly on top of it). Data from 500Å A-phase CaF_2 devices showed currents that were many orders of magnitude below the currents of the 100Å and 200Å CaF_2 devices, perhaps indicating that if the current transport in the thinner CaF_2 layers is due to line defects, that these do not form across a 500Å layer, but do across a 100Å or 200Å layer. Assumptions made in the theoretical tunneling current model are a conduction band offset of 2.5eV between CaF_2 and Si, and an effective mass of 0.02 for electrons in CaF_2 (this choice is somewhat arbitrary; however the situation does not improve by picking a larger effective mass value. One reference¹⁹ places an upper limit on m in CaF_2 of 0.2). The calculations involve the use of a

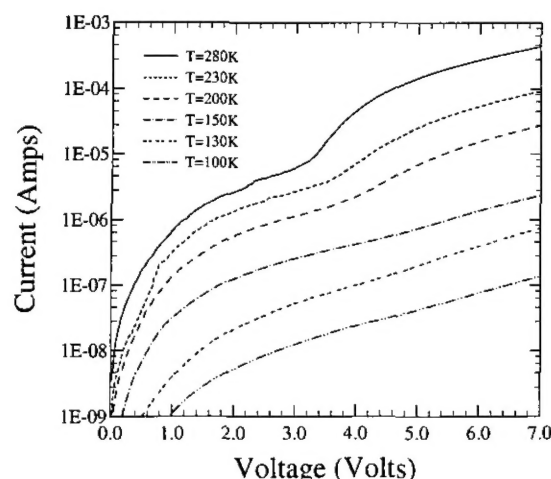


Figure 6: Current versus voltage characteristics of a 100Å A-phase CaF_2 barrier, with a single crystal top Si layer, at various temperatures.

three band model (one band for each layer), thus taking into account the effective mass discontinuity at the Si/ CaF_2 interface. This model ignores the depletion/accumulation effects on the conduction band, and is used only to determine the magnitude of current for varying barrier thickness.

Another series of devices were fabricated in a 100Å A-phase CaF_2 barrier structure that was grown with a single crystal silicon top layer. The current versus voltage and temperature characteristics for a 100Å A-phase Si/ CaF_2 /Si structure is shown in Figure 6. Ideally, transport through the barrier should be governed by direct tunneling at low applied voltages, and Fowler-Nordheim tunneling at higher voltages, where the discontinuity in the current versus voltage curve marks the crossover between these two regimes. However, variable temperature measurements detailed below indicate that this kind of transport is not occurring in our devices.

As can be seen in Figure 6, the higher bias regime has a much different temperature dependence than that of the lower bias regime. This should not be the case if transport is occurring via tunneling through an epitaxial layer of CaF_2 . The only temperature dependence in the tunneling current will come from the number of electrons at a given temperature available to tunnel, given by

$$N(T) = 2 \left(\frac{2\pi m_a^* kT}{h^2} \right)^{3/2} M_C \exp \left(\frac{-(E_C - E_F)}{kT} \right) \quad (1).$$

Since at a given temperature the electrons, $N(T)$ is a constant, changes of $N(T)$ that are temperature induced will affect both direct tunneling and Fowler-Nordheim tunneling in the same way. Therefore, they should both

have approximately the same temperature dependence. As is seen in Figure 6, the two regions above and below ~3.5 Volts have very different temperature dependences, with the higher voltage region decreasing much more rapidly in current than the lower voltage region.

A subsequent fabrication of these devices was identically done, except that now a 1000Å indium layer was deposited on top of the aluminum contact. During biasing of the device, it was observed that in the higher bias regime, voids in the indium layer formed on the order of one per every $900\mu\text{m}^2$. This value is consistent with the value seen in the previous 100Å A-phase CaF_2 devices. These appear to be formed due to electromigration of indium, most likely caused by locally high current densities through pin-hole defects in the CaF_2 layer. Thus, conduction through this 100Å CaF_2 layer sample is most likely through pin-hole defects.

4. Conclusions

We have fabricated thin Si/ CaF_2 /Si junctions in both A and B phase CaF_2 . It has been shown that the electrical properties of A-phase CaF_2 barriers are superior to those of B-phase CaF_2 , most likely due to fewer occurrences of defects in the growth of A-phase CaF_2 . However even in the A-phase material studied, conduction through the CaF_2 layer is dominated by conduction through defects. Current versus voltage and temperature characteristics of CaF_2 samples grown with a single crystal Si top layer, as well as studies employing an indium top metal contact, were also supportive of transport through defects.

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